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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,439	12/28/2001	Eleanor P. Rabadam	42P12399	8983

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EXAMINER
LEE, EUGENE

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,439	RABADAM ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second wire bond electrically coupling at least a portion of the passive component to the integrated circuit die must be shown or the feature(s) canceled from the claim(s). See claim 10. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4 thru 10, and 13 thru 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Spielberger et al. '778. Spielberger discloses (see, for example, Figure 5) a memory device comprising a chip (integrated circuit die) 40b and capacitor (passive device) 60. In column 3, lines 12-21, Spielberger states that chips may be memory chips. Regarding claims 2, 4, and 7, see column 4, lines 40-42 wherein Spielberger states that a chip is bonded by a conductive or nonconductive adhesive, and column 4, lines 12-17 wherein Spielberger states that epoxies are examples of adhesives. Regarding claim 6, see package (substrate) 14b. Regarding

claim 8, see wires (first wire bond) 28a on the left side of the device shown in Figure 5. Regarding claims 9 and 10, see the other wires (second wire bond) 28a on the right side of device shown in Figure 5.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spielberger '778. Spielberger discloses the claimed invention except for the epoxy material between the passive component and the integrated circuit die being less than about 0.050 millimeters in thickness. However, it was well known in the art at the time of invention to use this thickness in order to reliably attach one semiconductor component to another component in a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use an epoxy material being less than about 0.050 millimeters in thickness, in order to reliably attach the chip to the capacitor in Speilberger's invention, and since it has been held that discovering an optimum value of a result effective value involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spielberger et al. '778 as applied to claims 1, 2, 4 thru 10, and 13 thru 17 above, and further in view of Javanifard et al. '033 B1. Spielberger does not disclose the integrated circuit die including a flash memory

array. However, it was very well known in the art that flash memory arrays were one of many types (i.e. EEPROM, EPROM, SRAM, DRAM) of memory arrays utilized in memory chips. Javanifard discloses (see, for example, column 6, lines 9-15) a memory circuit device comprising one of these memory arrays, a flash memory. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a flash memory in Spielberger's device in order to utilize another common memory array that capably reads, writes, and stores data.

7. Claims 12, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spielberger et al. '778 as applied to claims 1, 2, 4 thru 10, and 13 thru 17 above, and further in view of Figueroa et al. '743 B1. Spielberger does not disclose a voltage regulator coupled to the integrated circuit die, wherein at least a portion of the voltage regulator is mounted to the integrated circuit die. However, Figueroa discloses (see, for example, column 1, lines 25-28) a voltage regulator providing a steady DC voltage in an integrated circuit package. Figueroa further states (see, for example, column 9, lines 33-37) that a voltage regulated power supply may be mounted on an IC package. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to mount a voltage regulator on the chip of Speilberger in order to supply a constant DC voltage to the chip.

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spielberger et al. '778 in view of Figueroa et al. '743 B1 as applied to claims 12, 18 and 19 above, and further in view of Sundstrom '177. Spielberger does not disclose a wire bond to electrically couple at least one passive component and the integrated circuit. However, it was extremely well known in the art at the time of invention to use wires to connect components of a semiconductor device.

Sundstrom teaches (see, for example, FIG. 3) a semiconductor device comprising a passive device 12 and an underlying die 10. A bonding wire 28 couples the passive device to the die 10. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a bonding wire in order to couple the voltage regulator and chip of Spielberger in view of Figueroa together.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
February 23, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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